

### **III. Remarks**

Claims 1-20 were originally filed in the present application. Claims 1-3 and 18-20 are presently cancelled without prejudice or disclaimer, and no other claims are presently amended or added. Accordingly, claims 4-17 remain pending in the present application.


Claim 1 was rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. No. 6,571,371 to Coss, et al. ("Coss"). Claims 2, 3 and 18-20 were also rejected under 35 U.S.C. §103(a) as being unpatentable over Coss. However, while Applicants do not necessarily agree with these rejections, claims 1-3 and 18-20 are presently cancelled without prejudice or disclaimer, solely in an effort to expedite prosecution.

The Examiner also indicated that claims 4-17 are allowed. However, because the Examiner has not provided a statement of reasons for allowance, Applicants assume claims 4-17 are allowed because the prior art fails to teach or suggest a method of manufacturing semiconductor device gate dielectrics, comprising: cleaning a first substrate surface during a first time period; forming a first insulating layer over the first substrate surface during a second time period subsequent to the first time period; cleaning a second substrate surface during a third time period; and forming a second insulating layer over the second substrate surface during a fourth time period subsequent to the second and third time periods, wherein the third time period includes a cleaning delay period prior to a cleaning portion of the third time period, the cleaning delay period configured such that an end time of the third time period substantially coincides with a start time of the fourth time period.

Because all pending claims are allowed, Applicants respectfully request a notice of allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

  
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